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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,104	07/30/2003	Etsuko Terasawa	81754.0095	1911

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,104	TERASAWA ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-15 and 18-23* is/are rejected.

7)☒ Claim(s) *7,8,16,17,24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/30/05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-6, 9-15 and 18-23 are rejected under 35 U.S.C. 102(b) as being unpatentable by Itoh (US Patent 6,099,578).

2. As to claims 1, 9, 10 and 18 Itoh discloses:

(1), (9), (18) A method/program for designing a semiconductor device comprising:

receiving a net list of a semiconductor device (relation of connections between a macro cells and a nets on a semiconductor integrated circuit) (col.4, ll.56-59);

temporarily (initially) locating (positioning/placing) a plurality of functional blocks (subcircuits/circuits/modules) within a layout area of the semiconductor device (col.4, ll.53-55; col.5, ll.40-47; col.12, ll.44-50);

dividing a logic area of the semiconductor device into a plurality of rectangular areas (creating routing grid) (col.3, ll.33-41; col.6, ll.26-47);

computing a predicted value of a utilization rate (V4: Aluminum wiring grid occupation) of the logic area (V1:Area of placement and wiring) and a predicted value of a wiring length of the semiconductor device (V3: Total estimated wire length of the

circuit) based on a data base regarding a semiconductor device designed previously and the semiconductor device and the net list of the semiconductor device (col.6, ll.11-67; col.7, ll.1-15; col.10, ll.41-67; col.11, ll.1-20);

locating, dividing and computing when the predicted value of the utilization rate of the logic area of the semiconductor device does not satisfy a predetermined condition (col.1, ll.19-25; col.12, ll.10-32);

outputting floor plan information for allocating the plurality of functional blocks basic cells (macro cells) and wiring within the logic area of the semiconductor device when the predicted value of the utilization rate of the logic area satisfies the predetermined condition (col.12, ll.43-49); and

outputting the predicted value of the wiring length of the semiconductor device (col.11, ll.35-53);

(10) An apparatus for designing a semiconductor device comprising:

means for inputting a net list of a semiconductor device and information that designates an arranged location of a plurality of functional blocks, which are located within the semiconductor device (col.4, ll.53-59; col.5, ll.40-47; col.12, ll.44-50);

means for recording the net list of the semiconductor device (col.4, ll.56-67; col.5, ll.1-3; col.10, ll.15-40);

means for recording a data base with respect to a semiconductor device designed previously and the semiconductor device (col.4, ll.56-67; col.5, ll.1-3; col.10, ll.15-40);

means for recording information with respect to a basic cell located within the semiconductor device designed previously and the basic cell possibly located in a logic area of the semiconductor device (col.4, ll.56-67; col.5, ll.1-3; col.10, ll.15-40);

means for temporarily arranging the plurality of functional blocks, which temporarily arranges the plurality of functional blocks within a layout region of the semiconductor device, in response to information designating the arranged location (col.4, ll.53-55; col.5, ll.40-47; col.12, ll.44-50);

means for dividing the logic area of a semiconductor device into a plurality of rectangular areas (col.3, ll.33-41; col.6, ll.26-47);

means for computing a predicted value of a utilization rate of the logic area, which computes a predicted value of a wiring length and the predicted value of the utilization rate of the logic area of the semiconductor device based on the data base and the net list of the semiconductor device (col.6, ll.11-67; col.7, ll.1-15; col.10, ll.41-67; col.11, ll.1-20);

a means for judging the predicted value of the utilization rate of the logic area, which judges whether the predicted value of the utilization rate of the logic area in the semiconductor device satisfies a predetermined condition or not, and promoting a user to input information designating new arranged location for the plurality of functional blocks located within the semiconductor device when the predicted value of the utilization rate of the logic area does not satisfies the predetermined condition (col.1, ll.19-25; col.12, ll.10-32);

means for outputting floor plan information, which outputs floor plan information for arranging the plurality of functional blocks, basic cells, and wiring within the logic area of the semiconductor device or arranges the plurality of functional blocks, basic cells, and wiring when the predicted value of the utilization rate of the logic area satisfies the predetermined condition (col.12, ll.43-49);

means for outputting the predicted value of the wiring length, which outputs the predicted value of the wiring length of the semiconductor device (col.11, ll.35-53); and

means for displaying the layout of the semiconductor device where the plurality of functional blocks is temporarily arranged by the means for temporarily arranging a plurality of functional blocks an image for promoting the user to input information designating new arranged location for the plurality of functional blocks located within the semiconductor device when the predicted value of the utilization rate of the logic area does not satisfy the predetermined condition; and/or the layout of the semiconductor device where the plurality of functional blocks, basic cells, and wiring are arranged by the means for outputting floor plan information (col.1, ll.19-25; col.4, ll.56-67; col.5, ll.1-3; col.12, ll.10-32; col.12, ll.43-49).

3. As to claims 2-6, 11-15 and 19-23 Itoh recites:

(2), (11), (19) The method/apparatus/program of designing a semiconductor device further comprising: producing the data base including information regarding a basic cell, information regarding a net list, information regarding a wiring length, information regarding a utilization rate of the logic area (col.4, ll.56-67; col.5, ll.1-3; col.10, ll.15-40);

(3), (12), (20) The method/apparatus/program of designing a semiconductor device, wherein, the information regarding the basic cell includes information regarding a number of pins held by the basic cell, information regarding a number of nets connected to the basic cell (col.7, ll.15-51);

(4), (5), (13), (14), (21), (22) The method/apparatus/program of designing a semiconductor device, wherein the information regarding the basic cell includes information regarding a relationship between the net list and the number of pins, which is obtained by classifying all nets in terms of a connection pin number (col.7, ll.15-51; col.12, ll.6-9; col.9, ll.36-42);

(6), (15), (23) The method/apparatus/program of designing a semiconductor device, wherein information regarding the utilization rate includes a maximum value (col.3, ll.33-41; col.6, ll.26-47; col.10, ll.15-41).

Allowable Subject Matter

4. Claims 7-8, 16-17 and 24-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

The method of designing a semiconductor device further comprising:

producing a first equation for computing a predicted value of an average value of the wiring length of a total number of nets for the semiconductor device, a second

equation for computing a gradient in a graph where a number of connecting pins is along the abscissa and a predicted value of an average value of the wiring length of a net for every number of connecting pins along the ordinate, or a third equation for computing a predicted value of an average value of the wiring length of the net of which the number of connecting pins within the net of the semiconductor device is two "2", based on the data base, in response to a number of layers of aluminum wiring layers of the semiconductor device; producing a fourth equation for computing the predicted value of the utilization rate of the logic area of the semiconductor device based on: the data base; the predicted value of the average value of the wiring length of the total number of nets of the semiconductor device; the gradient in the graph where the number of connecting pins is along the abscissa and the predicted value of the average value of the wiring length of the net for every number of connecting pins along the ordinate with respect to the total number of nets of the semiconductor device; or the predicted value of the average value of the wiring length of the net of which the number of connecting pins within the net of the semiconductor device is two "2" that were computed in the previous step (i); and the total number of nets of the semiconductor device in response to the number of layers of aluminum wiring layers of the semiconductor device; a step (l) computing the predicted value of the utilization rate of the logic area of the semiconductor device based on the fourth equation, in response to the number of layers of aluminum wiring layers of the semiconductor device; and a step (m) correcting the predicted value of the utilization rate of the logic area of the semiconductor device in response to the configuration of the rectangular area.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Naum Levin

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Naum Levin

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